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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Berthold et al.

MMB Docket No. **1890-0052**

Application No. **10/774,349**

Filed: **February 6, 2004**

For: **Method for a Parallel Production of an MOS Transistor and a Bipolar Transistor**

Examiner: **To be assigned**

Group Art Unit: **2812**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

September 20, 2004
(Date of deposit)

James D. Wood
Name of person mailing Document or Fee

Signature

September 20, 2004
Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicants hereby disclose the following references regarding the above-identified patent application. Copies of the foreign documents are enclosed.

Patent References

U.S. Patent No.	Inventor	Issue Date
5,354,699	Ikeda et al.	October 11, 1994
5,641,692	Miwa et al.	June 24, 1997
5,824,560	Van Der Wel et al.	October 20, 1998
6,103,560	Suzuki	August 15, 2000
6,440,787 B1	Yoshihisa	August 27, 2002

Foreign Application	Issue Date	Country
JP 2001203288	July 27, 2001	Japan
WO 96/30940	October 3, 1996	PCT
WO 96/30941	October 3, 1996	PCT
EP 0 851 486 A1	December 16, 1997	Europe
EP 0 746 032 A2	December 14, 1995	Europe
JP 2000-40758	February 8, 2000	Japan
JP 63244768	October 12, 1988	Japan
JP05 006961A	January 14, 1993	Japan

Articles

1) English Translation of Abstract for Japanese Publication No. 63244768.

2) English Translation of Abstract for Japanese Publication No. 2001203288.

3) English Translation of Abstract for Japanese Publication No. 05 006961A.

4) "Technologie hochintegrierter Schaltungen", Widmann, Mader, Friedrich ("0,7 µm-BICMOS-Prozeß"), pps 319-335, (17 pages).

U.S. Patent No. 6,440,787 B1 is an English language equivalent of JP 2001203288.

US 6,103,560, US 5,354,699, US 5,824,560, JP 2001-203288, and EP 746 032 were cited in the National German Examination Procedure in a related German patent application number 101 38 648.6 filed on August 7, 2001.

EP 0 851 486, WO 9630941, WO 9630940, JP 05 006961, and US 5,354,699 were cited in an International Preliminary Examination Report (English translation enclosed) in a related PCT patent application number PCT/EP02/07312 filed on July 2, 2002. Additional references were cited in the Preliminary Search Report for the PCT patent application (copy enclosed) and/or the Preliminary Search Report for another related PCT patent application number PCT/EP02/07313 filed on July 2, 2002.

Japanese Publication No. 2000-40758 discloses a method for producing MOS transistors and bipolar transistors. On a surface of a silicon substrate, electrodes are structured in a MOS region and electrodes are structured in a bipolar region. Sidewalls are generated at lateral surfaces of the structured electrodes which are subsequently removed in order to perform a doping of the drain and source portions.

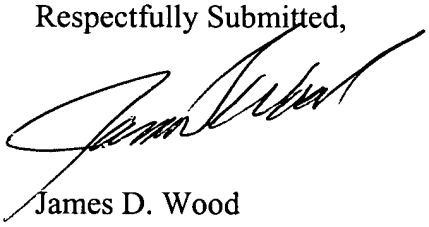
Technologie hochintegrierter Schaltungen discloses a BICMOS process wherein a substrate is doped by iron implantation in order to produce conductive regions in the substrate. A silicon layer is produced after doping the substrate whereon a $SI_3 N_4$

material is deposited on the silicon oxide layer. The $SI_3 N_4$ layer is etched in order to allow a local oxidation whereafter the layer s removed. Collector terminals are produced by iron implantation via a structured photo resist layer. The photo resist layer is removed and a second photolithographic process using a second mask is performed in order to define the base zone of the bipolar transistors. The second photo resist layer is removed and a gate oxide is generated for the MOS transistors. A polysilicon gate layer is deposited and a further mask is used in order to define the gate. The source and drain regions are doped by iron implantation whereafter an isolating oxide layer is generated in order to produce the dielectric layer of a capacitor. A second polysilicon layer is deposited for generating of the capacitor and high resistance resistors. The second polysilicon layer is etched to structure this polysilicon layer and a silicon oxide etching is performed in order to generate contact holes. A metal is deposited and etched in order to contact active regions of the device.

Pursuant to 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed within three months after the filing date of the application or before the mailing of the first office action on the merits.

It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

Respectfully Submitted,



September 20, 2004
Maginot, Moore & Beck
Bank One Center Tower
111 Monument Circle, Suite 3000
Indianapolis, Indiana 46204-5115
(317) 638-2922

James D. Wood
Attorney for Applicants
Registration No. 43,285

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0052	APPLICATION NO.: 10/774,349
	APPLICANT(S): Berthhold et al.	
	FILING DATE: February 6, 2004	GROUP ART UNIT: 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	5,354,699	October 11, 1994	Ikeda et al.			
	AB	5,641,692	June 24, 1997	Miwa et al.			
	AC	5,824,560	October 20, 1998	Van Der Wel et al.			
	AD	6,103,560	August 15, 2000	Suzuki			
	AE	6,440,787 B1	August 27, 2002	Yoshihisa			
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL	JP 2001203288	July 27, 2001	Japan			Yes No
	AM	EP 0 746 032 A2	December 14, 1995	Europe			Yes No
	AN	WO 96/30940	October 3, 1996	PCT			Yes No
	AO	WO 96/30941	October 3, 1996	PCT			Yes No
	AP	EP 0 851 486 A1	December 16, 1997	Europe			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	1	English Translation of Abstract for Japanese Publication No. 63244768.
	AR	1	English Translation of Abstract for Japanese Publication No. 2001203288.
	AS	1	"Technologie hochintegrierter Schaltungen", Widmann, Mader, Friedrich ("0,7 µm-BICMOS-Prozeß"), pps 319-335, (17 pages).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.

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	BA						
	BB						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	BL	JP05 006961A	January 14, 1993	Japan			Yes No
	BM	JP 63244768	October 12, 1988	Japan			Yes No
	BN	JP 2000-40758	February 8, 2000	Japan			Yes No
	BO						Yes No
	BP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
	BQ	2	English Translation of Abstract for Japanese Publication No. 05 006961 A.
	BR	2	
	BS	2	

EXAMINER	DATE CONSIDERED

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